National Semiconductor
The Sight & Sound of Information

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DP83849CVS-EVK Purpose and Contents

The purpose of the DP83849CVS-EVK (EVK) is to provide National Semiconductor Corp.'s customers with a vehicle to quickly design and market systems containing the DP83849CVS. Customers are encouraged to copy EVK components to expedite their design process.
The EVK contains:

- DP83849 Demo II board
- Printed copy of this User's Guide
- DP83849 Demo II schematic
- DP83849 Demo II licensing agreement

Information and Specifications

This section contains specifications of the DP83849 Demo II board, as well as a description of the board's interfaces, connectors, jumpers and LEDs.

Usage setup and configuration

Power for the DP83849 is supplied through the MII connector or via a POE Power Supply Equipment (PSE) device through the RJ-45 connector for **PORT A**, pins: (+) for 1, 2, 4, 5 and (-) for 3, 6, 7, 8.

1. ***MII connection:***
   Need to install J8, J10, and J92.

   For MII with 5V supply: Need to install J23. A voltage regulator, U3, will convert the MII 5V connection to 3.3V for the device.

   For MII with 3.3V supply: Remove J23. No voltage regulator is used; supply is connected to 3.3V plane via J92 for the device.

2. ***PSE device through pins:*** (+) for 1, 2, 4, 5 and (-) for 3, 6, 7, 8 *of J85 (RJ-45 connector for PORT A).* A separate daughter board with POE circuit is required to connect to the POE connector, J91. The module will detect and convert the voltage to 3.3V for the device. Need to populate 0 ohm resistors (R226, R227, R228, and R229). Remove J8, J23, and J92.

   Require a separate baby board that connects to the POE connector, J91.

   Note: Only use **PORT A** for PSE connection. Operation has been proven with 48V @ 4A supply when R161, R162, R163, R164 are 75 ohm resistors while powering through pins: (+) 4,5 and (-) 7,8.

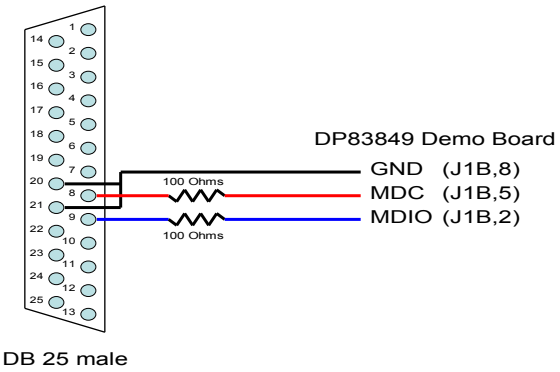
3. ***External 3.3V power supply****:* Remove jumper J92 and use pin 1, labeled as 3V3, for (+) plus and pick the nearest ground pin for (-) connections.

To access the device registers

1. ***Access MDIO through SmartBits with one of the ports:***
   Add jumpers to J1 pins (1-2, 4-5, 7-8) for access through PORT A.
   Add jumpers to J1 pins (2-3, 5-6, 8-9) for access through PORT B.

2. ***Access MDIO with Parallel Cable (In Line Resistors):***
Require the installation of Integrity Utility Software v3.24 or higher and the use of a parallel cable. One side connects to the parallel port of a PC and the other end directly to the device signals: MDIO (J1B,2), MDC (J1B,5), and GND (J1B,8) as shown in Figure 1. Jumpers at J1 and J26 must be removed.

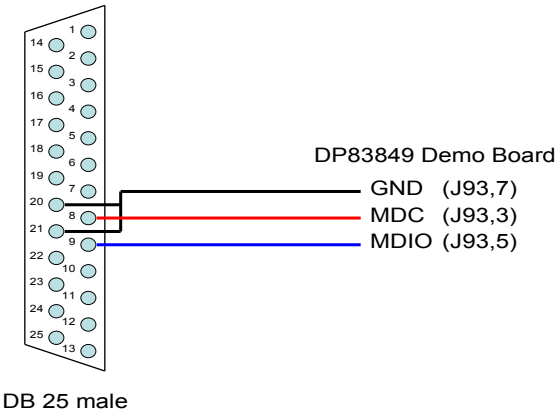
Figure 1. Direct Connect Cable with In Line Resistors



3. ***Access MDIO through the Integrity Interface, J93, with Parallel Cable:***
Require the installation of Integrity Utility Software v3.24 or higher and the use of a parallel cable. One side connects to the parallel port of a PC and the other end directly to the device signals: MDIO (J93,5), MDC (J93,3), and GND (J93,7) as shown in Figure 2.

Remove U4, U5, U6, C111, C112, C113, R232, and replace R233 with 100 Ohms.
Short the following pins: U4 (pins 2&4), U5 (pins 1&4), U6 (pins 3&4).
Add jumpers to J26 (1-2, 3-4). Remove all jumpers at J1.

Figure 2. Direct Connect Cable without Resistors



LED options:

PORT A: Add jumpers to J45 pins 1-2 for **LINK**, J46 pins 1-2 for **SPEED**, J47 pins 1-2 for **ACT/COL**
PORT B: Add jumpers to J44 pins 1-2 for **LINK**, J43 pins 1-2 for **SPEED**, J42 pins 1-2 for **ACT/COL**
The datasheet should be referenced for specific LED settings.

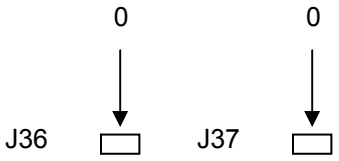
Address settings:

The PMD address for the DP83849 Physical Layer device is set by jumpers J36 and J37.

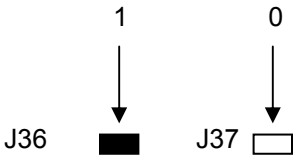
- Default board setting for **PORT A** is PHY Address 0 and **PORT B** is PHY Address 1
- The board may be set to other PHY Addresses as noted in the diagrams below:

Setting jumpers to High = 1 

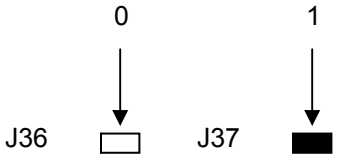
Setting jumpers to Low = 0 



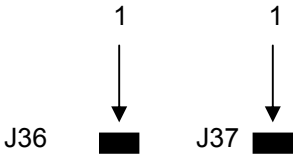
PORT A = PHY Address 0
PORT B = PHY Address 1



PORT A = PHY Address 2
PORT A = PHY Address 3



PORT A = PHY Address 4
PORT B = PHY Address 5



PORT A = PHY Address 6
PORT A = PHY Address 8

Alternative clock source:
There are two options to choose: Oscillator and Crystal.

1. On this board, a 25 MHz crystal is used as clock input for the device in MII configuration.
2. To use with 25 MHz oscillator, populate R225 with 0 ohm resistor, remove the crystal and C35.
3. To use with 50 MHz oscillator in RMII configuration, populate R223 and R224 with 22 ohms resistor, populate R225 with 10 ohm resistor, and remove the crystal along with C35.

Option for RMII configuration:

Populate R110 and R112 with 0 ohm resistors to enable RMII mode for both ports: A and B.
Use 50 MHz clock source as stated above.

Table of jumpers:

Jumper	Name	Function	Setting
Power			
J8	MII 5V/3V3	Select 5V or 3.3V from MII connector	Jumpered
J10	MII port selection	Select MII voltage from Port A/B	Jumpered
J23	3V3 _LP3964	Use 3V3 from the voltage regulator	Jumpered
J91	POE Connector	Allow 48Vfrom a PSE. Requires a separate baby board.	Open
J92	MII_3V3	Enable voltage from MII to the board	Jumpered
Reset			
J4	RESET_N	Allow external RESET	Open
MDIO/MDC Access			
J1	MDIO/MDC	Allow MDIO/MDC signals connect from MII (SmartBits) to Port A/B	Jumpered
J26	uMDIO	Allow the Integrity Interface connect to the device.	Open
Address			
J36	PHYAD1	Phy Addresses strap pin	Open
J37	PHYAD2	Phy Addresses strap pin	Open
Auto-Negotiation			
J42	ANEN_B	Port B – Enable/Disable Auto Negotiation	Jumpered
J43	AN1_B	Port B – Forced/Advertised Operation Mode in Auto Negotiation	Jumpered
J44	AN0_B	Port B – Forced/Advertised Operation Mode in Auto Negotiation	Jumpered
J45	AN0_A	Port A – Forced/Advertised Operation Mode in Auto Negotiation	Jumpered
J46	AN1_A	Port A – Forced/Advertised Operation Mode in Auto Negotiation	Jumpered
J47	ANEN_A	Port A – Enable/Disable Auto Negotiation	Jumpered
Function			
J40	EXTENDER_EN	Allow Extender Mode (For DP83849IVS/IFVS)	Open
J41	CLK2MAC_DIS	Disable Clock to MAC output	Jumpered
J48	PWRDOWN_INT_B	Port B – Allow Power Down and Interrupt Mode	Open
J49	ED_EN_B	Port B – Enable Energy Detect Mode	Open
J50	FX_EN_B	Port B – Enable Fiber Mode (For DP83849IDVS/IFVS)	Jumpered
J51	MDIX_EN_B	Port B – Enable/Disable MDIX Mode (Default is Enabling)	Open
J52	LED_CFG_B	Port B – Allow LEDs configuration. See datasheet	Open
J55	LED_CFG_A	Port A – Allow LEDs configuration. See datasheet	Open
J56	MDIX_EN_A	Port A – Enable/Disable MDIX Mode (Default is Enabling)	Open
J57	ED_EN_A	Port A – Enable Energy Detect Mode	Open
J58	PWRDOWN_INT_A	Port A – Allow Power Down and Interrupt Mode	Open
Interface			
J2	JTAG pins	JTAG interface (For DP83849IVS/IDVS/IFVS)	
J7	MII Header	Port B – Allow connection to MII pins	
J9	MII Male Connector	Port B – SmartBits interface	
J13	MII Header	Port A – Allow connection to MII pins	
J14	MII Male Connector	Port A – SmartBits interface	
J84	Connector	Port B – RJ-45 connector	
J85	Connector	Port A – RJ-45 connector	
J89	FX transceiver	Port B – HP FX transceiver (HFBR5803). Not stuffed in copper configuration	
J90	CLK2MAC	Clock output. Not stuffed	
J93	Integrity Interface	Allow access to the device with National Integrity Software	

Additional information for all options above may be found in the DP83849IVS datasheet.

DP83849 Demo II Specification

Overview

The DP83849 Demo II is a National Semiconductor demo platform to allow customer evaluation of our device. While the DP83849 has many advanced and enticing features, this specific board is designed to demonstrate *only* a subset of those. The features chosen are the ones that the mainstream customers will use. Thus we have created an affordable, aesthetic platform to demonstrate the simplicity of designing in a National Semiconductor DP83849.

Target Environment

Equipment that provides standard IEEE 802.3 MII, RMII or SNI interface; e.g. SmartBits/Netcom

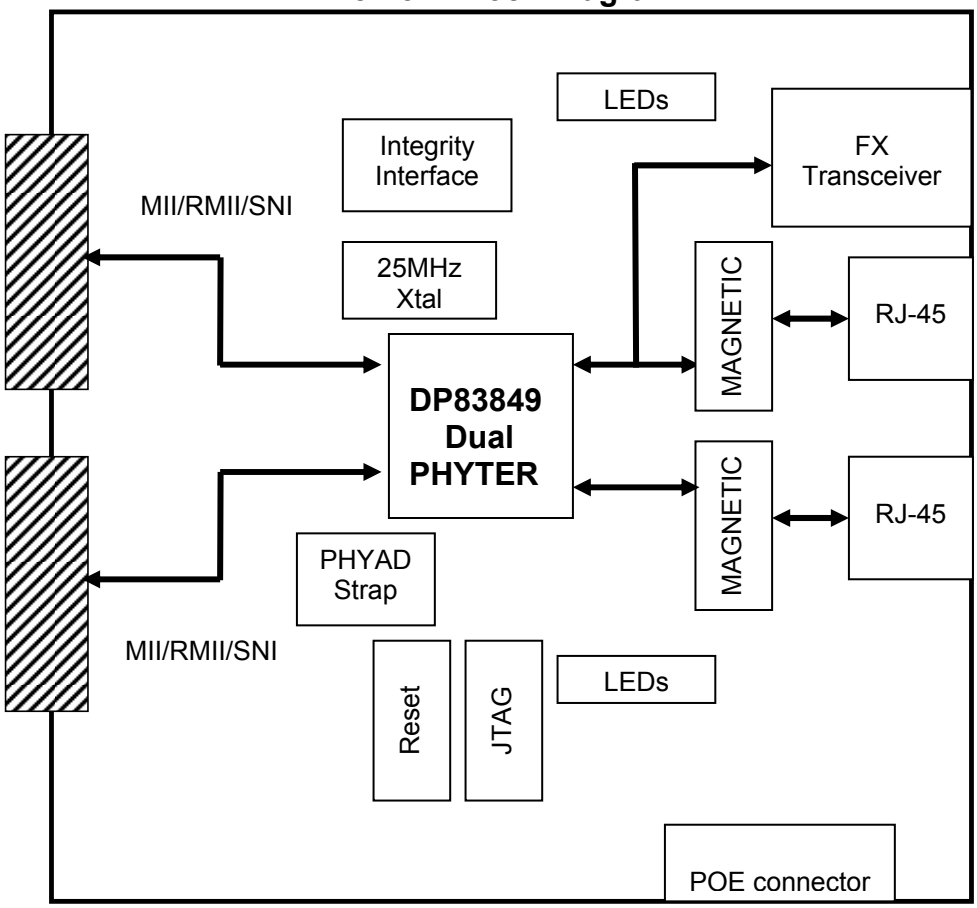
Features/Goals

The DP83849 Demo II features:

- Multiple PHY Addresses – Default are 00h (Port A), 01h (Port B) with increment even values through 30h (Port A) and odd values through 31h (Port B).
- 9 LEDs – 1 power, 2 INTERRUPT, 6 others (2 LINK, 2 SPEED, 2 ACT/COL) dependant on LED mode selected
- Strap Options for Ports (A and B) – ED_EN, MDIX_EN, LED_CFG, Auto-Negotiation
- FX_EN jumper - Port B only
- SNI_MODE resistor – Work with MII_MODE pin to set 10 Mb SNI mode. See Strap Options of datasheet for details.
- MII_MODE resistor – To set RMII mode. See Strap Options section of datasheet for details.
- EXTENDER_EN jumper – To set into Extender mode that DP83849IVS and DP83849IFVS support. See each datasheet respestively for details.
- CLK2MAC_DIS jumper – To disable clock to MAC output.
- RESET_N jumper – To allow external reset.
- PWR_DWN/INT jumper – To set the device into Interrupt mode.

- Connections for the following interfaces:
  - MII Interface
  - 2 x RJ-45, 1 x FX (Port B)
  - Header for “ribbon cable” connection to MII/RMII/SNI
  - JTAG header
  - CLK2MAC header
  - Integrity Interface header
- Standard PCB layout considerations with regards to clock, MII, and TD/RD
- On-board clock – Crystal/Oscillator Dual Footprint – 25/50 MHz
  - Crystal (default) – Should be depopulated for RMII option.
  - Oscillator – Resistor stuff option for RMII to bring in external 50 MHz oscillator
- On-board power supplied by 5V/3V MII connector (A/B), or POE connector (J91)
- Dual sided component placement
- Low cost

Demo II Block Diagram



PCB Physical Layout

- FR4 material
- Trace impedance Differential impedance 100 ohms, +/- 5%
- Uniform supply & ground plane
- 5.875" (height) 5.25" (length)
- 4 layers
- Combination of through-hole and surface mount technology

Demo II Interface requirements

- System interface will be via the MII connector, or MII/MRII/SNI header
- RJ-45 for network connection
- JTAG access via 2x5 header
- On Board Serial Management Circuit

Demo II Performance

The DP83849 Demo II supports line speed Ethernet network communications.
Signal quality, which affects IEEE compliance, can vary depending on board layout, power supplies, and components used, esp. isolation magnetics.
This reference design was NOT designed for operation over extreme temperature ranges.

Software

- No device specific software is required for this board
  National does provide the integrity utility; a diagnostic and configuration package at
  www.national.com/appinfo/networks/ethernet_utility.html

Additional information

Updated versions of the included material, related material can be found by going to
ethernet.national.com
or directly to design resources at
www.national.com/appinfo/networks/webench/DP83849.html

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